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Design of High Speed Low Power Reversible Logic Adder Using HNG Gate

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Abstract
Reversibility plays a fundamental role when computations with minimal energy dissipation are considered. In recent years, reversible logic has emerged as one of the most important approaches for power optimization with its application in low power CMOS, optical information processing, quantum computing and nanotechnology. This research proposes a new implementation of adder in reversible logic. The design reduces the number of gate operations compared to the existing adder reversible logic implementations. So, this design gives rise to an implementation with a reduced area and delay. We can use it to construct more complex systems in nanotechnology.
Keywords: Adder, Decimal Arithmetic, Reversible logic, Garbage output, HNG gate

I. INTRODUCTION

Energy loss during computation is an important consideration in low power digital design. Landauer's principle states that a heat equivalent to kT*ln2 is generated for every bit of information lost, where 'k' is the Boltzmann's constant and T' is the temperature . At room temperature, though the amount of heat generated may be small it cannot be neglected for low power designs. The amount of energy dissipated in a system bears a direct relationship to the number of bits erased during computation. Bennett showed that energy dissipation would not occur if the computations were carried out using reversible circuits since these circuits do not lose information. A reversible logic gate is an n-input, n-output (denoted as n*n) device that maps each possible input pattern to a unique output pattern. There is a significant difference in the synthesis of logic circuits using conventional gates and reversible gates. While constructing reversible circuits with the help of reversible gates fan-out of each output must be 1 without feedback loops. As the number of inputs and outputs are made equal there may be a number of unutilized outputs called garbage in certain reversible implementations. This is the number of outputs added to make an n-input k-output function reversible.

For example, a single output function of 'n' variables will require at least n-1 garbage outputs. Classical logic gates such as AND, OR, and XOR are not reversible. Hence, these gates dissipate heat and may reduce the life of the circuit. So, reversible logic is in demand in power aware circuits. A reversible conventional adder was proposed using conventional reversible gates.

A Full adder design using two types of reversible gates - NG (New Gate)and NTG (New Toffoli Gate) with 2 garbage outputs was implemented. The BCD adder was then designed using such full adders. Even though the implementation was improved in using TSG reversible gates, this approach was not taking care of the fanout restriction of reversible circuits, and hence it was only a near-reversible implementation. An improved reversible implementation of decimal adder with reduced number of garbage outputs is proposed.

Another improved reversible implementation of decimal adder using reversible gates which results in further reduction in number of gates and garbage outputs with a fanout of 1 is proposed in fig9. The present work proposes a modified version of decimal addition using reversible gates which results in reduction in number of gate operations in full adder reversible gates with a fanout of 1.

II. LITERATURE SURVEY

Energy loss is an important consideration in digital circuit design. A part of this problem arises from the technological non ideality of switches and materials. The other part of the problem arises from Landauer's principle for which there is no solution. **Landauer's Principle states that logical computations that are not reversible necessarily generate k*T*ln (2) joules of heat energy, where k is the Boltzmann's Constant k=1.38xlO-23 J/K, T is the absolute temperature** at which the computation is performed. Although this amount of heat appears to be small, Moore's Law predicts exponential growth of heat generated due to

information lost, which will be a noticeable amount of heat loss in next decade. **Also by second law of thermodynamics any process that is reversible will not change its entropy.** On thermo dynamical grounds, the erasure of one bit of information from the mechanical degrees of a system must be accompanied by the thermalization of an amount of k*T*ln (2) joules of energy. The information entropy H can be calculated for any probability distribution. Similarly the thermodynamic entropy S refers to thermodynamic probabilities specifically. Thus gain in entropy always means loss of information, and nothing more. Design that does not result in information loss is called reversible. It naturally takes care of heat generated due to information loss. Bennett showed that zero energy dissipation would be possible only if the network consists of reversible logic gates, Thus reversibility will become an essential property in future circuit design technologies.

III. REVERSIBLE LOGIC

Reversible logic is a promising computing design paradigm which presents a method for constructing computers that produce no heat dissipation. Reversible computing emerged as a result of the application of quantum mechanics principles towards the development of a universal computing machine. Specifically, the fundamentals of reversible computing are based on the relationship between entropy, heat transfer between molecules in a system, the probability of a quantum particle occupying a particular state at any given time, and the quantum electrodynamics between electrons when they are in dose proximity. The basic principle of reversible computing is that a bi-jective device with an identical number of input and output lines will produce a computing environment where the electrodynamics of the system allow for prediction of all future states based on known past states, and the system reaches every possible state, resulting in no heat dissipation A reversible logic gate is an N-input N-output logic device that provides one to one mapping between the input and the output. It not only helps us to determine the outputs from the inputs but also helps us to uniquely recover the inputs from the outputs. Garbage outputs are those which do not contribute to the reversible logic realization of the design. Quantum cast refers to the cost of the circuit in terms of the cost of a primitive gate. Gate count is the number of reversible gates used to realize the function. Gate level refers to the number of levels which are required to realize the given logic functions.

The following are the important design constraints for reversible logic circuits.

I. Reversible logic gates do not allow fan-outs.

2. Reversible logic circuits should have minimum quantum cost.

3. The design can be optimized so as to produce minimum number of garbage outputs.

4. The reversible logic circuits must use minimum number of constant inputs.

5. The reversible logic circuits must use a minimum logic depth or gate levels.

The basic reversible logic gates encountered during the design are listed below:

1. **Feynman Gate :**

It is a 2x2 gate and its logic circuit is as shown in the figure. It is also known as Controlled Not (CNOT) Gate. It has quantum cost 1 and is generally used for Fan Out purposes.

2. **Peres Gate :**

It is a 3x3 gate and its logic circuit is as shown in the figure. It has quantum cost 4. It is used to realize various Boolean functions such as AND, XOR.

3. **Fred kin Gate :**

It is a 3x3 gate and its logic circuit is as shown in the figure. It has quantum cost 5. It can be used to implement a Multiplexer.

4. **HNG Gate :**

It is a 4x4 gate and its logic circuit is as shown in the figure. It has quantum cost 6. It is used for designing ripple carry adders. It can produce both sum and carry in a single gate thus minimizing the garbage and gate counts.

5.**Toffoli Gate :** The 3*3 Reversible gate with 3 inputs and 3 outputs. It has Quantum cost **5**

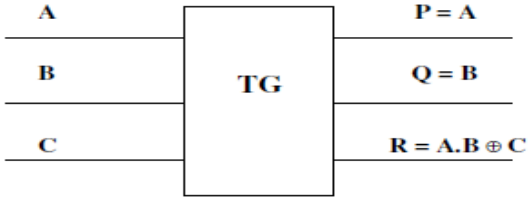
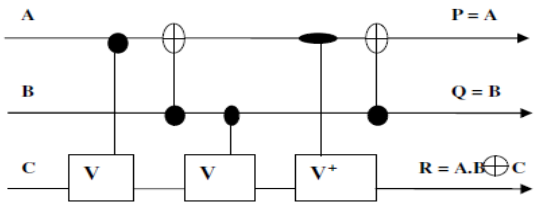


Figure 1. Toffoli gate



Quantum implementation of Toffoli gate

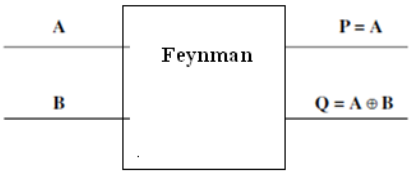
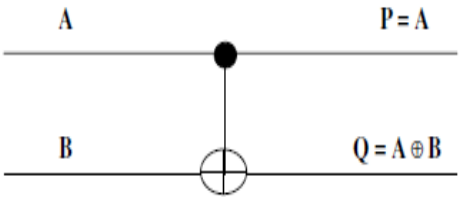


Figure 2. Feynman gate



Feynman/CNOT gate quantum implementatio

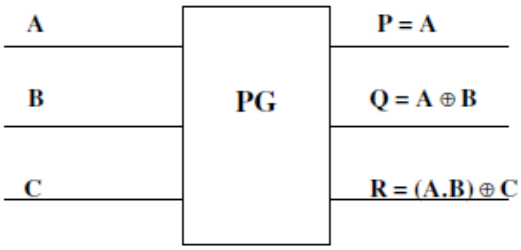
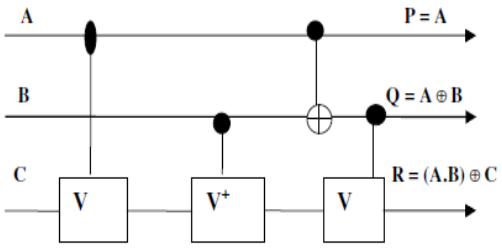


Figure 3. Peres gate



Quantum implementation of Peres gate

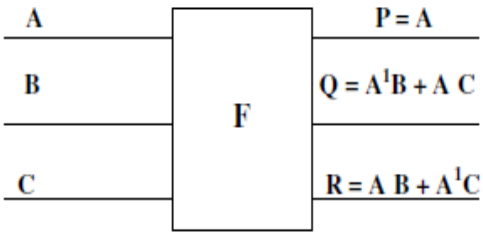
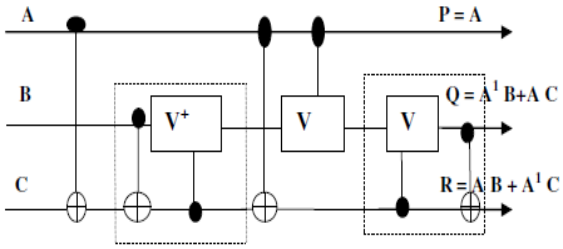


Figure 4. Fredkin gate



Quantum implementation of Fredkin gate

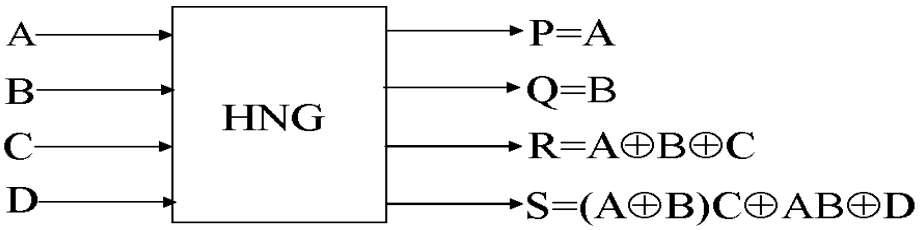
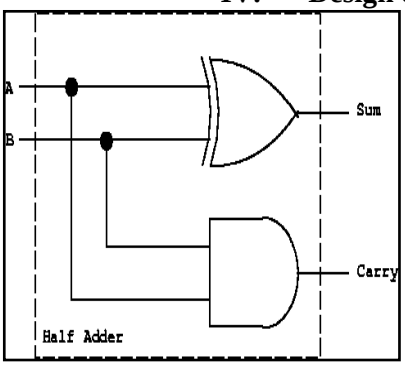


Figure 5. HNG gate

IV. Design of a Reversible Half-adder Circuit



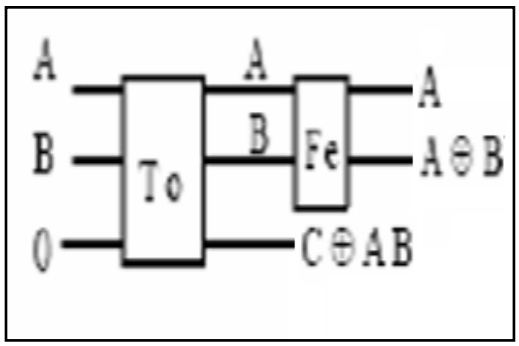


Figure 6.

V. Design of a Reversible Full-adder Circuit(cont.)

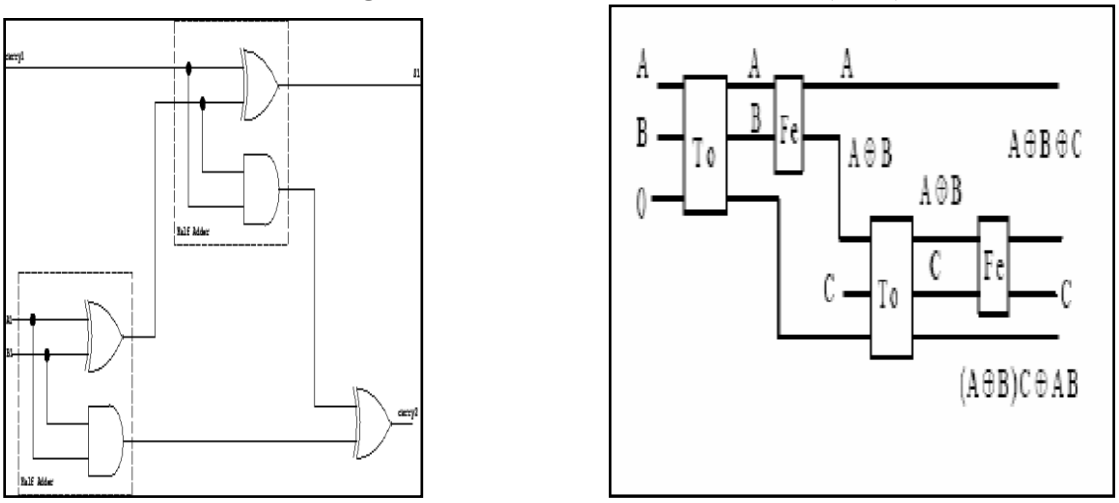


Figure 7.

VI. Existing Reversible Full-adder Circuits

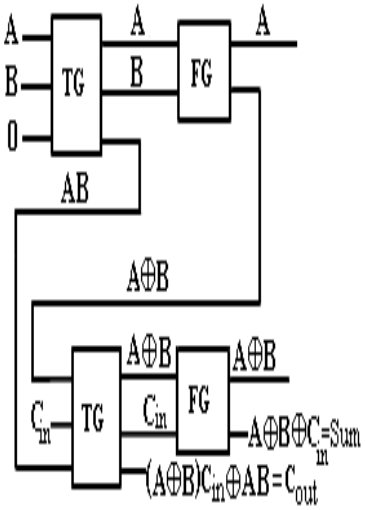
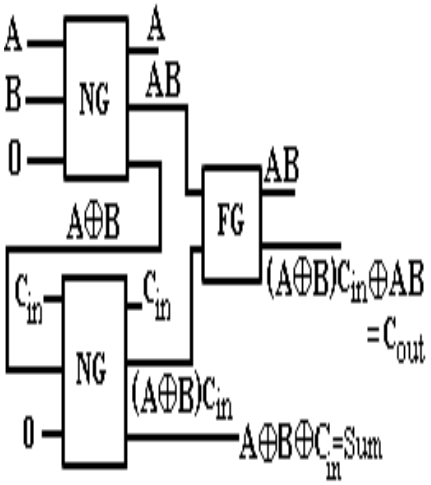


Figure 8. 4 gates and 2 garbage outputs



3 gates and 3 garbage outputs

VII. Proposed Reversible Full-adder Circuits

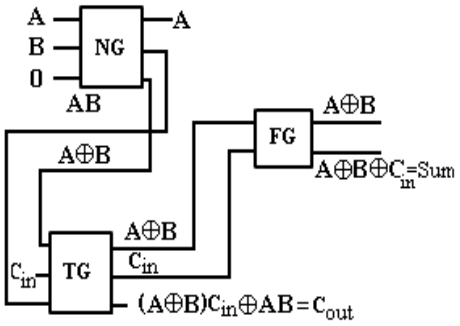
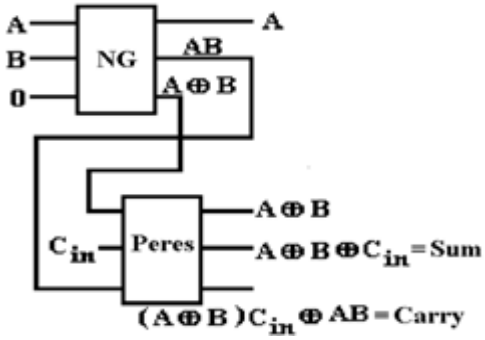


Figure 9. 3 gates and 2 garbage outputs



2 gates and 2 garbage outputs

VIII. Evaluation

The design of the reversible 4bit, 8bit, 16bit adder is logically verified using XILINX 8.1i and MODELSIM. The simulation results are as shown in figures.

Here we introduce a new function called the "Total Reversible Logic Implementation Cost (TRLlC)" which is defined as the sum of all the cost metrics of a given reversible circuit. The TRLIC can be deemed as a parameter which reflects the overall performance of a reversible logic circuit. TRLIC=∑(NG,CI,QC,GO) where NG is the number of gates in the reversible circuit.CI is the number of constant inputs, QC is the quantum cost of the circuit. GO is the number of garbage outputs. The following are the important design constraints for any reversible logic circuits.

I. Reversible logic circuits should have minimum quantum cost.

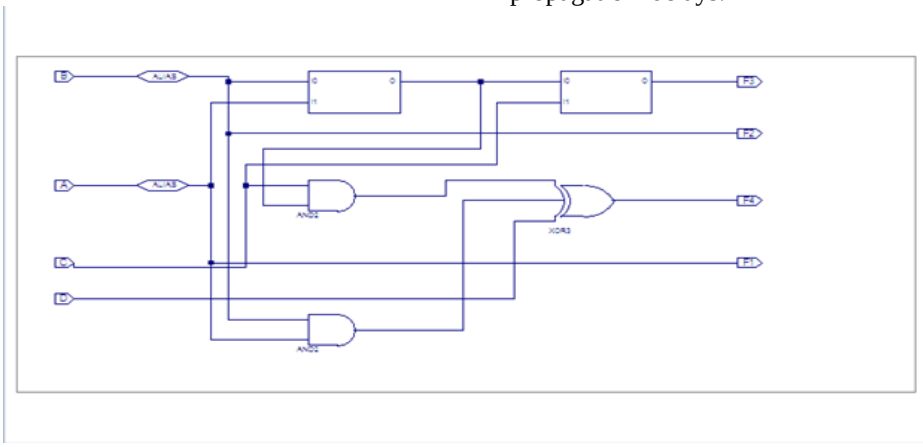
2. The design can be optimized so as to produce minimum number of garbage outputs.

3. The reversible logic circuits must use minimum number of constant inputs.

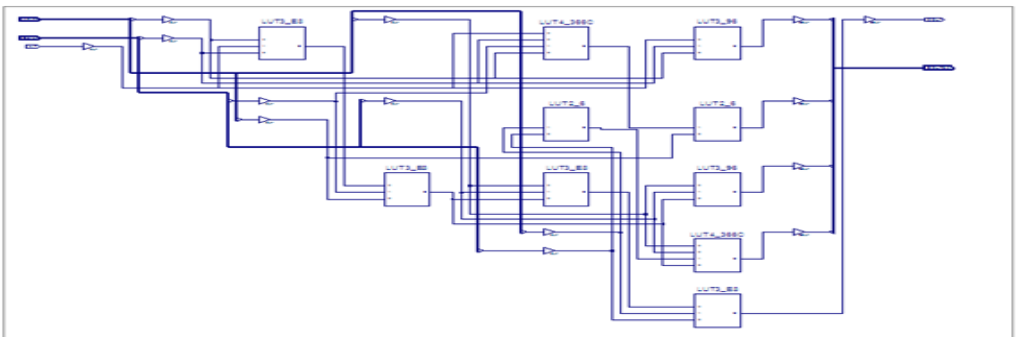
4. The reversible logic circuits must use a minimum number of reversible gates.

8.1. Simulation Methodology

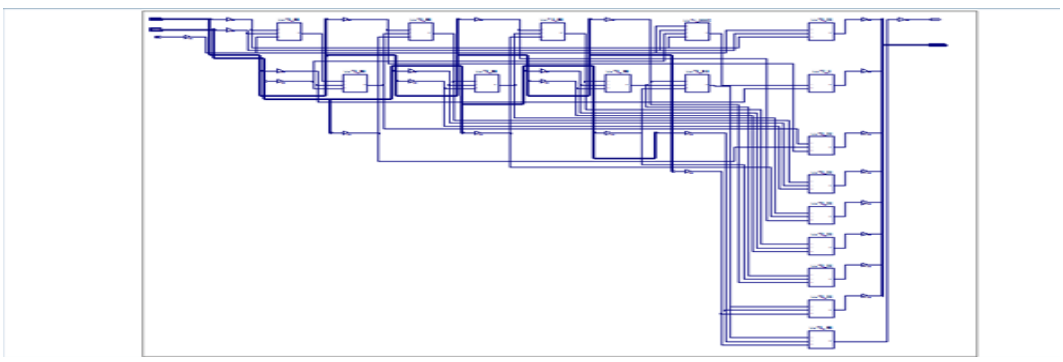
Xilinx 8.1i has been used to simulate the wave forms. The simulator carefully modeled the interconnections, the associated blocks and the propagation delays.



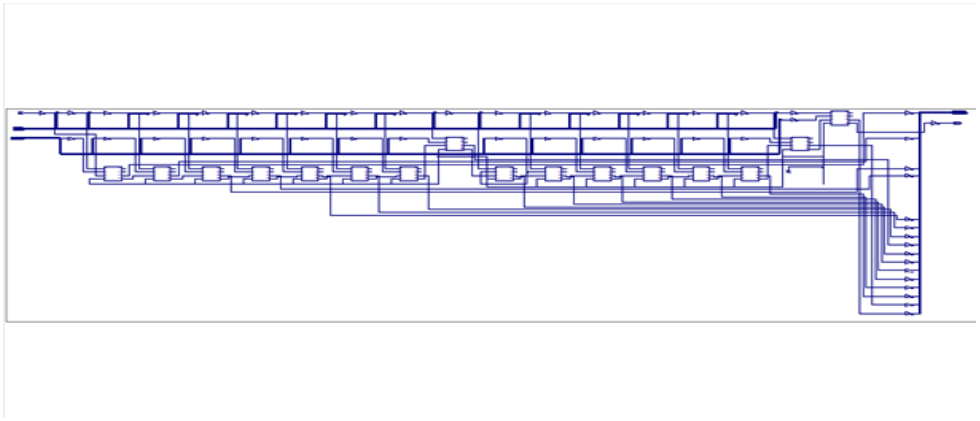
RTL SCHEMATIC OF HNG GATE



RTL SCHEMATIC OF 4 BIT ADDER USING HNG GATE



RTL SCHEMATIC OF 8 BIT ADDER USING HNG GATE

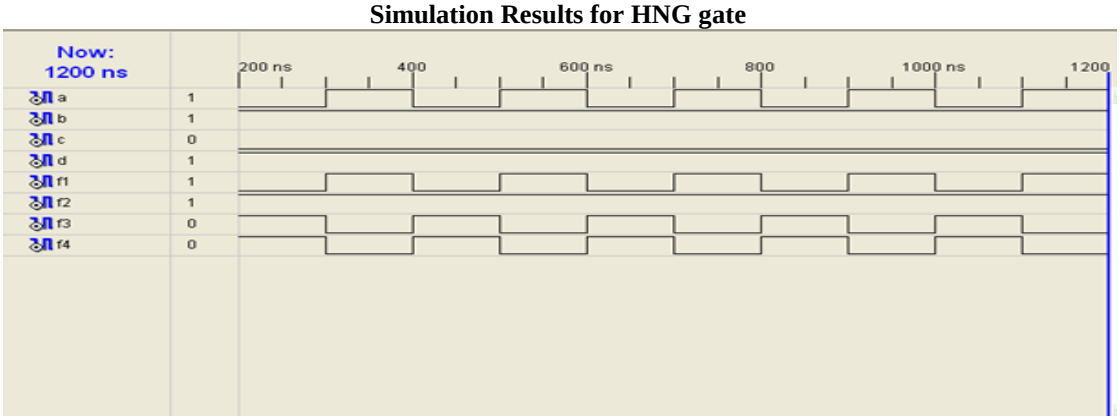


RTL SCHEMATIC OF 16 BIT ADDER USING HNG GATE

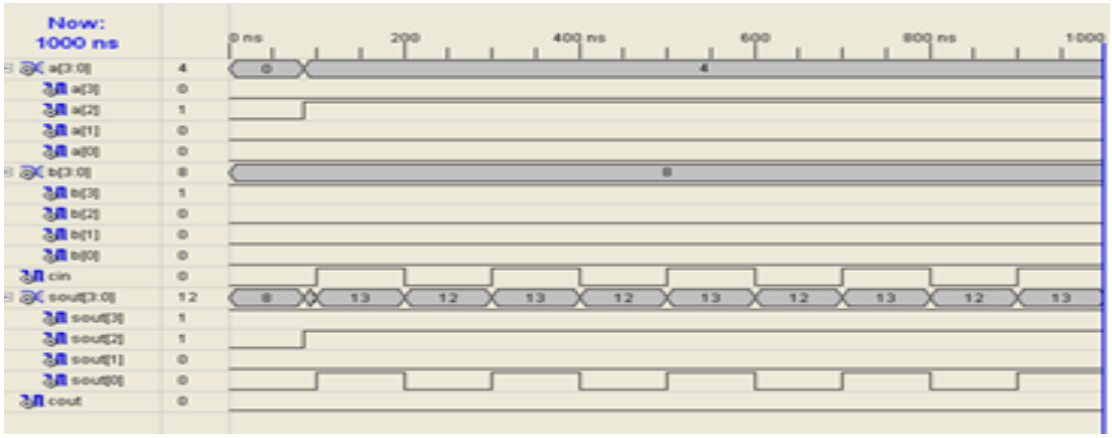
8.2.Results:

Reversible 4bit, 8bit, 16bit Adders are implemented using VHDL code and Simulated using Model sim Simulator. The overall logic is implemented using Structural style of Modeling and simulation results are shown in shown in Figure below-

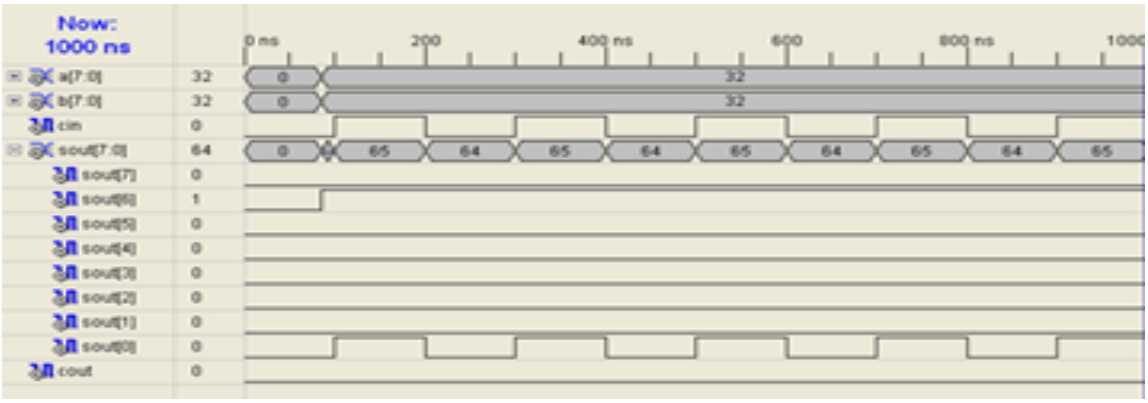
Simulation Results for HNG gate



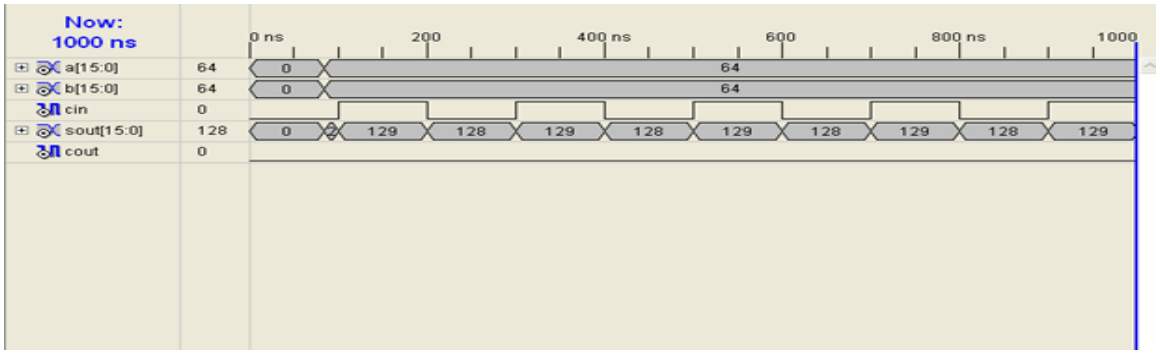
Simulation Results for 4 Bit Adder



Simulation Results for 8 Bit Adder



Simulation Results for 16 bit Adder



IX. Conclusion

The Reversible HNG gate are used to implement Adders . In this paper, we proposed Reversible 4bit, 8bit,16 bit Parallel Binary Adder unit. , these can be used for low power applications. In future, the design can be extended to any number of bits for Parallel Binary Adder unit and also for low power Reversible ALUs, Multipliers and Dividers.

References

[1] *R. Landauer, "Irreversibility and Heat Generation in the Computational Process", IBM Journal of Research Development, 5, 1961, 183-191.*

[2] *Bennett, C., "Logical Reversibility of Computation," IBM Journal of Research and Development, 17, 1973, 525-532.*

[3] *Hafiz Md. Hasan Babu and A. R. Chowdhury, "Design of a Reversible Binary Coded Decimal Adder by Using Reversible 4-bit Parallel Adder", VLSI Design 2005, pp-255-260, Kolkata, India, Jan 2005.*

[4] *Himanshu. Thapliyal, S. Kotiyal and M.B Srinivas, "Novel BCD Adders and their Reversible Logic Implementation for IEEE 754r Format", VLSI Design 2006, Hyderabad, India, Jan 4-7, 2006, pp. 387-392.*

[5] *R. James, T. K. Shahana, K. P. Jacob and S. Sasi,"Improved Reversible Logic Implementation of Decimal Adder", IEEE 11th VDAT Symposium Aug 8-11, 2007.*

[6] *Md. M. H. Azad Khan, "Design of Full-adder With Reversible Gates", InternationalConference on Computer and Information Technology, Bangladesh, 2002, pp. 515-519.*

[7] *R. Feynman, "Quantum Mechanical Computers", Optical News, 1985, pp. 11-20.*

[8] *H. Thapliyal and M.B Srinivas, "A Novel Reversible TSG Gate and Its Application forDesigning Reversible Carry Look-Ahead and Other Adder Architectures", Tenth Asia-Pacific Computer Systems Architecture Conference, Singapore, Oct 24 - 26, 2005*

[9] *Rekha K.james,Shahana T.K,T.Poulose Jacob,Sreela Sasi "A new look at Reversible logic implementation of Decimal adder",IEEE 1- 4244-1368-0/07.*

[10] *Jagadguru Swami Sri Bharati Krishna Tirthaji Maharaja, Vedic Mathematics: Sixteen Simple Mathematical Formulae from the Veda, Delhi (1965).*

[11] *Rakshith Saligram and Rakshith T.R. "Novel Code Converter Employing Reversible Logic", International Journal of*

Computer Applications (IJCA), August 2012.

[12] *Himanshu. Thapliyal ,K.p Jacob, Majid haghparast & Keivan Navi Design of High speed low power Reversible Logic BCD Adder Using HNG gate IEEE Transactions on VLSI Systems,March 2013.*

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Mr. Rajesh Khatri has 20 years of Teaching experience and presently working as Associate Professor in Department of Electronics & Instrumentation Engineering at SGSITS Indore. He received his Bachelor of Engineering in Electronics and Communication from SGGS Institute of Technology Nanded, India in 1990. He received his Master of Engineering in Instrumentation from SGGS Institute of Technology Nanded, India in 1995.